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A Hybrid Low Power Fast Full Adder Using XOR And XNOR Gates

R.K.Uma Maheswari[1#] , Dr.C.N.Marimuthu [2*]

[1#]PG Scholars, [2]* Professor & Dean, Department of Electronics and Communication Engineering, Nandha Engineering College (Autonomous), Erode, India

***Correspondence:** Dr.C.N.Marimuthu, Professor & Dean Department of Electronics and Communication Engineering Nandha Engineering College (Autonomous), Erode India. **E-Mail:** muthu_me2005@gmail.com, umahap@gmail.com

Abstract

In this paper, novel circuits for XOR/XNOR and simultaneous XOR–XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption and delay, which are due to low output capacitance and low short-circuit power dissipation. Many existing XOR-XNOR cells suffer from non full-swing outputs, high power consumption and low speed issues. In this paper, a new fast, full-swing and low-power XOR XNOR cell, is presented. In this paper, a hybrid 1-bit full adder design employing both complementary metal–oxide–semiconductor (CMOS) logic and transmission gate logic is reported. The design was first implemented for 1 bit and then extended for 32 bit also. We also propose six new hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR–XNOR or XOR/XNOR gates. Each of the proposed circuits has its own merits in terms of speed, power consumption, power delay product (PDP), driving ability, and so on. To investigate the performance of the proposed designs, extensive HSPICE and Cadence Virtuoso simulations are performed. The simulation results, based on the 65-nm CMOS process technology model, indicate that the proposed designs have superior speed and power against other FA designs.

Keywords: exclusive-OR(XOR),exclusive-NOR(XNOR) full-swing, high-speed, low-power, Fulladder (FA)

Introduction

Today, ubiquitous electronic systems are an inseparable part of everyday life. Digital circuits, e.g., microprocessors, digital communication devices, and digital signal processors, comprise a large part of electronic systems. As the scale of integration increases, the usability of circuits is restricted by the augmenting amounts of power [34] and area consumption. Full adders, being one of the most fundamental building block of all the aforementioned circuit applications, remain a key focus domain of the researchers over the year. Different logic styles, each having its own merits and bottlenecks, was investigated to implement 1-bit full adder cells. The designs, reported so far, may be broadly classified into two categories: 1) static style and 2) dynamic style. Static full adders are generally more reliable, simpler with less power requirement but the on chip area requirement is usually larger compared with its dynamic counterpart. Different logic styles tend to favor one performance aspect at the expense of others. Standard static complementary metal–oxide–semiconductor (CMOS), dynamic CMOS logic complementary pass-transistor logic (CPL) , and transmission gate full adder (TGA) are the most important logic design styles in the conventional domain.[12] The other adder designs use more than one logic style, known as hybrid-logic design style, for their implementation. These designs exploit the features of different logic styles to improve the overall performance of the full adder. In addition, full-adders are important components in other applications such as digital signal processing (DSP) architectures and microprocessor. Arithmetic functions such as addition, subtraction, multiplication and division are some examples which use adder as a main building block . In nano-scaling, the biggest power consumption is static power dissipation. Depending on the application, the kind of circuit implemented, and the design techniques used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles. The XOR-XNOR cells play a vital

role in numerous circuits such as adders, compressors, comparators, parity checkers and so on. Therefore, their behavior can affect the circuit performance greatly. The advantages of standard complementary (CMOS) style-based adders (with 28 transistors) are its robustness against voltage scaling and transistor sizing; while the disadvantages are high input capacitance and requirement of buffers. Another complementary type smart design is the mirror adder with almost same power consumption and transistor count but the maximum carry propagation path/delay inside the adder is relatively smaller than that of the standard CMOS full adder. On the other hand, CPL shows good voltage swing restoration employing 32 transistors [12]. However, CPL is not an appropriate choice for low-power applications. Because of its high switching activity of intermediate nodes (increased switching power), high transistor count, static inverters, and overloading of its inputs are the bottleneck of this approach. The prime disadvantage of CPL, that is, the voltage degradation was successfully addressed in TGA, which uses only 20 transistors for full adder implementation. However, the other drawbacks of CPL like slow-speed and high-power consumption remain an area of concern for the researchers. Later, researchers focused on the hybrid logic approach which exploited the features of different logic styles in order to improve the overall performance.

Previous works

One way is implementing XOR output, then turning it to XNOR output using an inverter. Two different designs that use this method are shown in Figs. 1(a) and 1(b) . Fig. 1(a) shows a circuit which uses low power XOR gate (LP-XOR) presented in to implement XOR function and a static CMOS inverter to implement XNOR function [23]. This circuit is characterized by its low power consumption [12]and uses only six transistors, but it has non full-swing outputs. In the case of input signals AB=00, both PMOS transistors before the inverter will be ON and a poor low signal will appear at the XOR output, i.e. PMOS threshold voltage (TP V). This weak signal can still drive the inverter and produce strong '1' at the XNOR output. In the other input combinations, the output signals will be complete. The other structure that uses an inverter to implement XNOR output from XOR output is illustrated in Fig. 1(b). This circuit uses two transmission gates and three inverters. Although the mentioned problem is fixed in this design, but the main drawbacks are high average power consumption and low speed [12]due to presence of three inverters. It is worth mentioning that delays of XOR and XNOR outputs of designs in Figs. 1(a) and (b) are different due to presence of an inverter for producing the XNOR output. Another way to realize XOR-XNOR functions is to generate them simultaneously as depicted in Figs. 1(c), (d) [4] and (e). The circuit in Fig. 1(c) is a low power design which is made of eight transistors and uses low power XOR and XNOR gates reported in to produce its both outputs simultaneously. This design does not provide full-swing outputs. When both inputs A and B are low, the XOR output has weak logic level (a little higher than 0, i.e. TP V), and when both are high, the XNOR output has weak logic level (a little lower than VDD, i.e. VDD – VTN). Therefore, the mentioned drawback of design in Fig. 1(a) exists as well. This problem will be more critical in submicron technologies and low supply voltages [23]. Two previously reported XOR-XNOR cells which produce both outputs simultaneously and provide good output levels in all possible input combinations are shown in Figs. 1(d), 1(e). To guarantee full-swing operation cross-coupled PMOS transistors are used in both circuits. Design in Fig. 1(e) is very similar to design in Fig. 1(d), except it uses only one inverter.

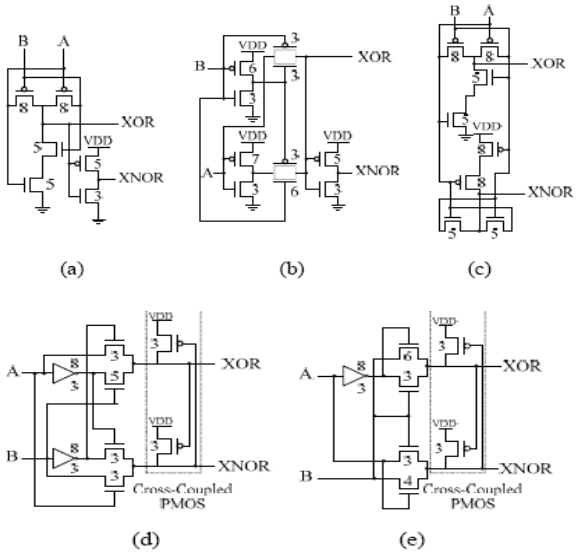

Fig.1. Five different design of XOR-XNOR circuit. (a)Wang`s circuit, (b) and (c) Shan`s circuit, (d)Aguirre`s circuit and (e) Goel's circuit

In this section we propose the design of a new XOR-XNOR cell that provides full-swing outputs simultaneously in all input combinations. But before going through the design procedure, we start with two new circuits for implementing XOR and XNOR gates separately as shown in Fig. 2. These circuits use one static CMOS inverter for implementing their function and both use only five transistors. Their most important drawback is the arrival of a bad logic level for one input combination at output nodes. In Fig. 2(a) when AB=00, transistor MN will be OFF, and both

transistors, MP1 and MP2 will be ON. Because of passing low logic value through PMOS transistors, threshold voltage of a PMOS transistor (TP V) will be produced at the XOR output. In the case of AB=11, for the circuit depicted in Fig. 2(b), transistor MP will be OFF and both NMOS transistors will be ON. Therefore high logic level passes through NMOS transistors and yields weak '1' at XNOR output. By combining circuits in Fig. 2(a) and (b). To overcome the problem of non full-swing outputs of designs shown in Fig. 2(a) and (b), a feedback loop consisting of one PMOS and one NMOS transistor is used. In the case of AB=00, first, weak '0' appears at XOR output, but it is still capable to turning the PMOS transistor in feedback loop (MPF) ON. Then VDD passing through this PMOS turns the NMOS transistor in feedback l (MNF) ON and produces strong '0' at XOR output. When both inputs are high, weak '1' appears at XNOR output In this case, MNF will be ON, passing '0' to XOR output, MPF will turn on and produces strong '1' at XNOR output. In the other input combinations, both outputs have full-swing voltages.

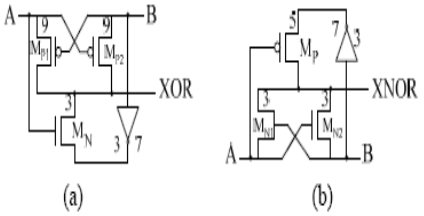

Fig.2. New design for XOR and XNOR gates. (a) XOR gate, (b) XNOR gate

Proposed Method

Proposed XOR–XNOR Circuit

The non full-swing XOR/XNOR circuit of Fig. 3(a) is efficient in terms of the power and delay [34]. Furthermore, this structure has an output voltage drop problem for only one input logical value. To solve this problem and provide an optimum structure for the XOR/XNOR gate, we propose the circuit shown in Fig. 3(b). For all possible input combinations ,the output of this structure is full swing. The proposed XOR/XNOR gate does not have NOT gates on the critical path of the circuit. Thus, it will have the lower delay and good driving capability in comparison with the structures of previous method. Although the proposed XOR/XNOR gate has one more transistor than the structure of previous one. It demonstrates lower power dissipation and higher speed[4] [34]. The input A and B capacitances of the XOR circuit shown in Fig. 3(b) are not symmetric, because one of these two should be connected to the input of NOT gates and another should be connected to the diffusion of nMOS transistor. Furthermore, the input capacitances of transistors N2 and N3 are not equal in the optimal situation (minimum PDP).Also, the order of input connections to transistors N2 and N3 will not affect the function of the circuit[34]. Thus, it is better to connect the input A, which is also connected to the NOT gates, to the transistor with smaller input capacitance. By doing this, the input capacitances are more symmetrical, and thus, the delay and power consumption of the circuit will be reduced. To clarify which transistor (N2 or N3) has larger input capacitance, let us consider the condition that the inputs change from AB = 00 to AB = 10.

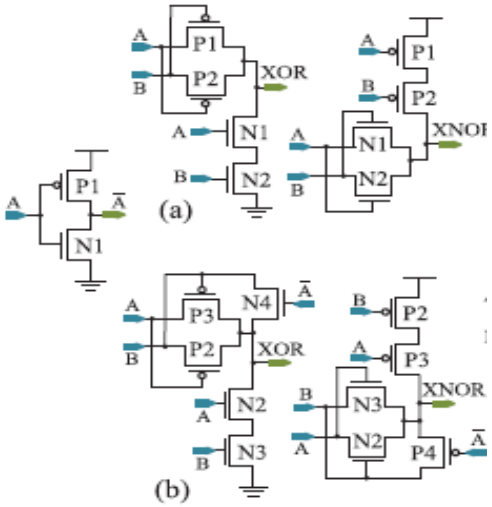

Fig.3(a)Non full-swing XOR/XNOR gate. (b) proposed full-swing XOR/XNOR gate.

Simulation environment

Simulation Setup

All the circuits have been simulated using HSPICE in the65-nm TSMC CMOS process technology, and were supplied with 1.2 V as well as the maximum frequency for the inputs was 1 GHz. Fig. 4(a) and (b) shows the typical simulation test bench to carry out the circuit parameters. There are two NOT gates on the input of structure shown in Fig. 4(a) with two separate power supplies (VDD1 and VDD2). As can be seen in Fig. 4(a), the main circuit and the NOT gates connected to it have the same power supply (VDD1). By subtracting the power consumption of VDD1 in Fig. 4(b) from the power consumption of VDD1 in Fig. 4(a), the power consumption of the main circuit will be achieved[4] [34] The input pattern for the both structures of Fig. 4(a) and (b) is exactly the same. With this method, the calculated power consumption of the main circuit will be much more accurate and the power consumption of

all input capacitance is also considered. Output load of FO4 is used for delay and power dissipation measurements, which has a different power supply from the main circuit. The sizes of input buffers are selected. In the output rise and fall transition, the delay is calculated from 50% of the input voltage level to 50% of the output voltage level[34]. The PDP will be calculated by multiplying the worst case delay by the average power consumption of the main circuit.

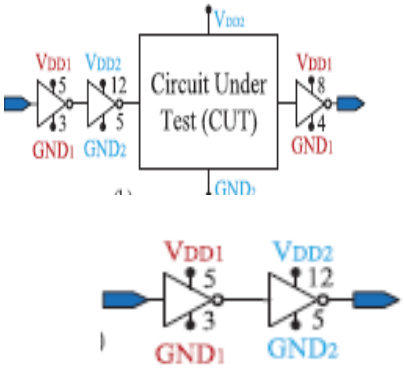

Fig.4.(a)&(b) Simulation test bench to carry out the circuit parameters.

Simulation power results

DESIGNS		POWER
Sham's circuit	Fig 1.b	1.04 µW
Aguirre`s circuit	Fig 1.d	1.13 µW
Goel's circuit	Fig 1.e	0.65 µW
Proposed full-swing XOR/ XNOR gate	Fig 3.b	2.22 mW

Conclusion

In this paper a new XOR-XNOR cell is designed and compared with previous works. Simulation results show that our proposed design has good functionality in 65-nm CMOS technology. In this paper, we first evaluated the XOR/XNOR and XOR–XNOR circuits. The evaluation revealed that using the NOT gates on the critical path of a circuit is a drawback. Another disadvantage of a circuit is to have a positive feedback on the outputs of the XOR–XNOR gate for compensating the output voltage level. This feedback increases the delay, output capacitance, and, as a result, energy consumption of the circuit. Then, we proposed new XOR/XNOR and XOR–XNOR gates that do not have the mentioned disadvantages.

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